WAFER-SCALE LASER PANTOGRAPHY: IV. PHYSICS OF DIRECT LASER-WRITING MICRON-DIMENSION TRANSISTORS

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ABSTRACT

The processes involved in the fabrication of micron-dimension transistors and small-scale integrated circuits using only the technique of direct laser-writing by localized pyrolytic surface reactions are discussed. New experimental findings in the deposition of tungsten by silicon surface reduction of tungsten hexafluoride and doped polysilicon are presented. The techniques used to fabricate laser beam-written n-MOSFET's are being extended to make unipolar JFET's and bipolar lateral pnp transistors.

INTRODUCTION

We recently reported[1] the ab initio fabrication of functional n-MOS field-effect transistors on a silicon wafer using only local laser-induced pyrolytic deposition, doping and etching reactions to effect the required semiconductor surface patterning. The laser pantographic techniques demonstrated in Ref. 1 can be readily applied to the fabrication of other unipolar (JFET) and also bipolar (lateral, vertical) transistors, to the repair of non-functioning units of complex integrated circuits, and to the multilayer interconnection of integrated circuit devices. Indeed, one subset of the latter capability was recently demonstrated[2] in the single layer interconnection of a CMOS gate array with laser beam-deposited doped polysilicon.

With control of the laser writing processes sufficient to optimize device quality and creation speed, these device fabrication, interconnection and repair techniques can be combined to usher in an era of rapid, high yield, discretionary fabrication of very complex circuits, such as customized supercomputers, on a single wafer. Clearly, timely attainment of such challenging goals requires a sufficient set of well-characterized and compatible direct laser beam-writing technologies. Several of those used to fabricate n-MOSFET's are further examined here. We are also currently using these laser direct-writing techniques to fabricate JFET's and bipolar lateral pnp transistors.

A sufficient set of laser processing steps for creating silicon-based unipolar and bipolar devices includes (selective) etching/deposition of insulators (SiO_2, Si_3N_4) for MOS gates and interconnect isolation; deposition (and etching) of doped polysilicon or doping pre-deposited silicon for gates, doped regions and interconnects for both unipolar and bipolar devices; and deposition of metals and metal silicides for interconnects and gates (W, WSi_2, Mo, Al, Au). Several of these steps have been demonstrated, such as etching of Si or SiO_2 with added HCl[1,3] or Cl_2[3] or, at times, in vacuum;[1] deposition of doped polysilicon with silane[1,4,5] laced with dopants (PH_3, B_2H_6),[1] and deposition of metal microstructures such as W (using $WF_6 + H_2$),[1,6] Ni (from $Ni(CO)_4$),[7,8] Al (from $Al(CH_3)_3$),[9] etc. Still, much needs to be learned about the electrical, structural, and adhesion properties of these (and other) laser beam-induced semiconductor modification processes.

In the laser beam-driven fabrication of n-MOSFETs,[1] a silicon wafer surfaced with a thermally grown silicon dioxide film was used as the input substrate. The focused laser locally milled away the oxide layer (and sometimes purposely some of

Mat. Res. Soc. Symp. Proc. Vol. 29 (1984) Published by Elsevier Science Publishing Co., Inc.

the underlying silicon) to pattern device source and drain regions, thereby demonstrating the compatibility of direct laser beam-writing with non-local processing.

Tungsten[10] and tungsten silicide[11] are very promising interconnect materials for next-generation VLSI/ULSI circuitry. The advantages of tungsten silicide include its low resistivity (compared to doped polysilicon), its high resistance to electromigration (compared to aluminum), and its ability to form a stable oxide. Pure tungsten has even better resistivity and electromigration properties than does tungsten silicide, though its oxide has poorer qualities. Consequently, laser-initiated deposition of W and WSi_2 are expected to be highly useful laser pantographic techniques, and deserving of further study.

Tungsten microstructures have previously been fabricated by hydrogen reduction of tungsten hexafluoride[1,6] on a laser-heated substrate:

$$WF_6 + 3H_2 \rightarrow W(s) + 6HF - 13\,\text{Kcal/mole (1300 K)} \quad (1)$$

An analogous process has been used to deposit tungsten on a non-locally heated silicon substrate[12,13] through reduction of WF_6 by the silicon surface:

$$WF_6 + \frac{3}{2}Si(s) \rightarrow W(s) + \frac{3}{2}SiF_4 + 171\,\text{Kcal/mole (1300 K)} \quad (2)$$

This reaction is intrinsically self-aligning on silicon and should produce superior ohmic contacts with better adhesion than those produced by the WF_6/H_2 reaction, since the WF_6 reacts with the atomically-bare silicon surface in reaction (2), while a tungsten deposit can also form on an impurity overlayer with reaction (1). With no added hydrogen, the thickness of the deposit, which is expected to be tungsten or tungsten silicide, is self-limited by the diffusion of WF_6 through the previously deposited molten or solid layers to fresh silicon surfaces. Thicker tungsten layers can then be made by adding hydrogen to the tungsten hexafluoride. The early results of a study of the formation of tungsten/silicon interfaces using local heating to drive the silicon reduction of tungsten hexafluoride are reported here.

As mentioned above, the deposition of doped polysilicon is an important step in many integrated circuit fabrication processes. A comprehensive study of the kinetics of the deposition of doped polysilicon and the electrical and materials properties of the deposit is underway. Some findings in the study of the deposition of phosphorous- and boron-doped silicon using PH_3/SiH_4 and B_2H_6/SiH_4, respectively, are presented here.

The laser direct writing processes which are used to create MOSFET's are also useful in generating unipolar junction field effect transistors (JFET's) and bipolar transistors. Use of local laser pyrolytic reactions to realize JFET and bipolar transistors with micron-scale channel length/base width is also discussed here.

EXPERIMENTAL APPARATUS

The laser microscope and overall experimental assembly in the present work are similar to those used in previous studies (Ref. 1, Figure 1; Ref. 7, Figure 2); the process-oriented microscope permits direct viewing of the vacuum chamber-positioned semiconductor substrate by a vidicon, and simultaneous irradiation by the laser beam focused onto the substrate. As in previous work, laser pulses are formed by electro-optically modulating the output of a CW argon-ion laser tuned to 5145 Å. These pulse sequences are coordinated with the x-y motion of the wafer-containing reaction chamber by computer control.

EXPERIMENTAL PROCEDURE AND RESULTS

Laser-Deposited Tungsten

In the tungsten deposition experiments, WF_6 at 100-1000 Torr pressures was introduced into a vacuum cell with a p-type (100), 40 Ω-cm silicon substrate that was degreased by solvents and treated with buffered HF to remove the native oxide layer. In the base case experiment, the wafer was mechanically scanned and the laser was electro-optically pulsed to give a single incident 100 μsec pulse for each sub-micron increment of wafer travel. The 5145 Å radiation incident on the target was focused by a 20×, N.A.=0.4 objective to a spot diameter ~2 μm.

The tungsten pads so deposited appeared shiny and much more reflective than the bare silicon substrate. Lines drawn under these conditions had widths $\lesssim$1 μm, as determined by scanning electron microscopy. Auger analysis was performed on the pads after various stages of sputtering. No fluorine ($\lesssim$1%) from the WF_6 was seen in any case examined. Small amounts of carbon and oxygen were observed near the surface, ascribed to handling and SEM analysis. As seen in Figure 1 (top) for the base case, the average thickness of the tungsten overlayer was ~180 Å (defined as the depth at which the tungsten atomic concentration is half the surface maximum). The Auger profile obtained with a total of two to five laser-overwriting scans on the same pad are essentially the same as with a single scan. Similar Auger profiles were observed with hydrogen added to the reaction gas mixture.

A significantly thicker tungsten deposit (~550 Å) in neat WF_6 was obtained when the laser pulse duration was increased to 500 μsec, as seen in Figure 1 (bottom). The surface layer in each case examined is apparently pure W with no contribution from tungsten silicide, WSi_2. The observed W/Si depth profile is, in part, due to the diffusion of WF_6 and W in the Si and, in part, to surface non-uniformities in deposition.

Laser-Deposited Doped Polysilicon

The reaction gases used in the doped polysilicon deposition experiments were vendor-supplied 1% B_2H_6/SiH_4 and 1% PH_3/SiH_4 mixtures, and samples further diluted in-house with silane. A thoroughly cleaned p-type (100), 6-9 Ω-cm silicon wafer with 1 μm thick silicon dioxide overlayer was the target substrate. The laser was focused (20× objective) at the Si-SiO_2 interface and not at the SiO_2-gas boundary. For resistivity measurements ~500 μm long, ~8 μm wide and ~1.5 μm thick lines were made, with four probing pads deposited at points appropriate for current and voltage measurements. Each line consisted of two laser-scans over the substrate. The transverse profile of each line was measured by profilometry.

Preliminary resistivity data is shown in Figure 2, plotted as a function of the B_2H_6/PH_3-to-SiH_4 ratio (upper ordinate scale) and also the polysilicon dopant concentration *assuming* molecular stoichiometric deposition (lower ordinate scale). Published curves of the resistivity of bulk p-type (boron) crystalline silicon[14] and high temperature (985°C) CVD p-type (boron) polycrystalline (~1 μm grain size)[15] vs. the boron concentration are displayed for reference. For phosphorus-doped material, the resistivity is nearly the same as for boron (~0.7× displayed crystalline value;[14] ~ same for polysilicon[16]). The resistivity of non-annealed silicon deposited by this (non-optimized) laser process is quite close to that of bulk CVD-deposited material.

SIMS analysis of these structures suggests that the P/Si doping ratio in the bulk of the deposited silicon pads using $[PH_3]/[SiH_4] = 10^{-2}$ may be only ~3 times larger than using $[PH_3]/[SiH_4] = 10^{-3}$. This could explain the flattening of the resistivity data for the phosphorous-doped structures in Figure 2.

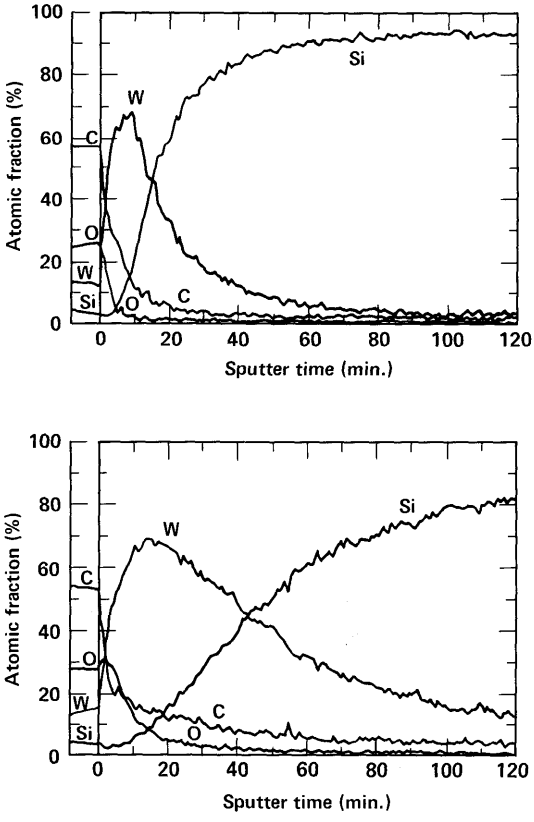

FIG. 1. Auger element analysis as a function of sputtering time for tungsten deposition from WF_6/Si(s) reactions. In the top curve 100 μsec long laser pulses were used (1 pulse per 0.1 μm travel), while 500 μsec pulses were used in the bottom curve. A sputter time of 10 minutes corresponds to removal of about 100 Å of material.

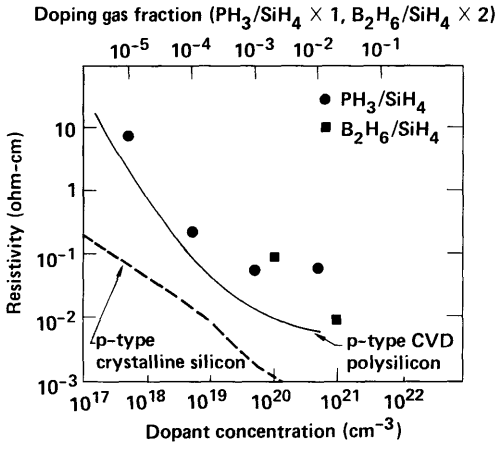

FIG. 2. Resistivity of laser-deposited doped polysilicion as a function of doping gas concentration (PH_3/SiH_4 × 1, closed circles; B_2H_6/SiH_4 × 2, plotted as closed squares). The lower ordinate axis converts this ratio to a silicon deposit doping level assuming equal rates of SiH_4, PH_3 and B_2H_6 surface decomposition. Also shown, are resistivity curves for p-type (boron) crystalline[14] (dashed line) and high-temperature CVD polycrystalline silicon[15] (solid line).

JFET/LATERAL PNP TRANSISTORS

A silicon-on-sapphire wafer (0.5 μm thick p-type Si, 3×10^{16} B atoms/cc) was laser beam-etched entirely through the silicon layer in the presence of HCl gas in order to electrically isolate the several transistor regions. Phosphorous-doped polysilicon was deposited across the width of the p-type island to form the gate of the (depletion-mode) junction field-effect transistor. Lateral pnp transistors were fabricated as were the JFET's, with additional heating to drive the phosphorous dopants all the way through the silicon layer, or by filling a laser beam/HCl-scribed trough between the collector and emitter regions of the moat-circumscribed boron-doped silicon regions with phosphorous-doped polysilicon. These procedures were sometimes followed by laser annealing of the entire base region.

Functional analysis of these devices is being performed.

CONCLUSIONS

We have previously reported the ab initio creation of MOSFET transistors via laser beam-energized, pyrolytically mediated patterning of the surfaces of silicon surfaces, and the interconnection of several such transistors to realize small scale integrated (SSI) circuits. The present paper reports on studies of the process physics underlying these earlier results, along with current work which is resulting in the direct laser-write creation of unipolar/bipolar transistors of two basic types, all with micron-scale minimum feature sizes.

The ability to synthesize MOSFET, JFET and lateral bipolar transistors with the same laser pantographic processes and techniques indicates that creation of wafer-scale integrated circuits containing intimate mixes of these different types of active devices (e.g., bipolar device-implemented logic elements in close proximity to FET-implemented memory cells) will be straightforward.

We expect that the laser beam-etched moat-and-island electrical isolation technique used in the bipolar transistor synthesis work, combined with the intrinsic advantages of shallow device structures created on insulating substrates, will prove to be a valuable and widely applicable approach in subsequent laser pantographic research.

ACKNOWLEDGMENTS

The authors wish to thank Dr. J. Balch for doping the silicon-on-sapphire substrates, D. Duerre, E. Ormsby, L. R. Mendonca and W. F. Gee for expert technical assistance throughout this work, and J. Trevino and J. Fischer for assisting with sample preparation and analysis.

Work performed under the auspices of the U.S. Department of Energy by the Lawrence Livermore National Laboratory under Contract W-7405-Eng-48.

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